We claim:

1. A method for performing an alignment measurement of two patterns in different layers on a semiconductor wafer, with a set of a fixed number of exposure fields selected for the alignment measurement, and with each of the exposure fields having at least one alignment structure, the method which comprises the following method steps:

providing the semiconductor wafer to a processing tool for performing the alignment measurement;

selecting a first alignment structure in a first exposure field of the set with the fixed number of exposure fields;

performing an offset measurement using the first alignment structure, and issuing an error signal if the offset measurement is not feasible due to a poor alignment structure quality or an offset lies beyond a tolerance range;

in response to the error signal, selecting a second exposure field as a substitute, wherein the second exposure field is not included in the set of exposure fields on the semiconductor wafer except for the first exposure field;

selecting a second alignment structure in the second exposure field;

performing an offset measurement using the second alignment structure; and

measuring a second relative offset of an alignment structure in a next exposure field of the set with the fixed number of exposure fields.

2. The method according to claim 1, wherein the second exposure field is the same as the first exposure field.

3. The method according to claim 1, wherein the second exposure field is different from the first exposure field.

4. The method according to claim 2, which comprises selecting the second alignment structure in the same exposure field, such that a relative distance between the first alignment structure and the second alignment structure is more than 10 microns and less than 100 microns.

5. The method according to claim 4, which comprises selecting the second alignment structure such that a dimension of a minimum linewidth thereof is different from a minimum linewidth of the first alignment structure by at least 20 percent.

6. The method according to claim 2, which comprises selecting the second alignment structure such that a dimension of a minimum linewidth thereof is different from a minimum linewidth of the first alignment structure by at least 20 percent.

7. The method according to claim 2, which comprises:

issuing an error signal when performing the offset measurement using the second alignment structure representing a case that the offset measurement either is not feasible due to a poor alignment structure quality or the offset measurement provides an offset beyond the tolerance range;

in response to the error signal, selecting a third exposure field as a substitute, wherein the third exposure field is not included in the set of exposure fields on the semiconductor wafer with the exception of the first exposure field; and

performing an offset measurement using a third alignment structure.

8. The method according to claim 1, wherein the processing tool is an exposure tool, and the alignment measurement is performed to provide a wafer stage adjustment.

9. The method according to claim 1, wherein the processing tool is an overlay metrology tool, and the alignment measurement is performed to control a quality of a recent manufacturing process carried out on the semiconductor wafer.

10. A method for performing a series of alignment measurements of each two patterns in different layers on a semiconductor wafer having a set of a fixed number of exposure fields selected for the alignment measurement, with each of the exposure fields having at least one alignment structure, the method which comprises:

training a neural network with the method steps of claim 1;

issuing a signal with the neural network in case an error signal is detected repeatedly in offset measurements in different layers for at least one exposure field of the semiconductor wafer; and

altering a selection of the set of exposure fields in response to the signal.